

SUBSTITUTE SPECIFICATION

STABILIZING COPPER OVERLAYER FOR ENHANCED C4 INTERCONNECT RELIABILITY

BACKGROUND OF THE INVENTION

Field of the Invention

The invention generally relates to interconnect structures of integrated circuits and more particularly to an improved interconnect structure that reduces the likelihood of voiding and delamination.

Description of the Related Art

The reduction of device dimensions and increased clock speeds strain the limits of today's C4 interconnect technology. The higher current densities required of next generation technologies increases the likelihood of voiding and delamination in the ball-limiting metallurgy (BLM) interconnect structure of solder joints due to atomic diffusion processes. This failure mode is especially rapid for systems employing solders with high concentrations of tin (Sn), such as the leading lead-free solders as well as eutectic PbSn solder.

More specifically, copper diffusion across the barrier layers when using such solders increases the likelihood of delamination. The solder bump BLM structures are susceptible to reliability failures in the ball-limiting metallurgy (BLM) when used to support tin-containing solders. In such situations, copper will diffuse through the barrier metallurgy and into the solder, leaving the layer of copper voided and depleted. This migration of the BLM copper is driven by the chemical potential gradient across the barrier layer. Elemental copper is unstable in the presence of tin, preferring to form intermetallic compounds such as Cu_3Sn or $\text{Cu}(\text{Ni})_6\text{Sn}_5$. The invention described below allows the use of such solders while substantially decreasing the likelihood of copper diffusion across barrier layers. Therefore, the invention substantially reduces the likelihood of voiding and delamination, which increases yield and reliability.

SUMMARY OF THE INVENTION

The invention provides an improved integrated circuit structure that has internal circuitry and interconnects (e.g. C4, etc.) on an external portion of the structure. With the invention, these interconnects have a metal layer on the external portion of the structure, a first copper layer on the metal layer, a barrier layer on the copper layer, a stabilizing copper layer on the barrier layer, and a tin-based solder bump on the barrier layer. The stabilizing copper layer has a sufficient amount of copper to balance the chemical potential gradient of copper across the barrier layer and prevent copper within the first copper layer from diffusing across the barrier layer. Alternatively, a sufficient amount of copper can be included within the tin-based solder bump to prevent copper from diffusing across the barrier layer. Thus, the tin-based solder bump

comprises a copper rich solder alloy. The metal layer comprises diffusion metallurgy including one or more of Al, Ti, TiW, Cr, Ta, and TaN. The barrier layer can be Ni, V, or NiV. The tin-based solder bump can be either a eutectic PbSn solder or a lead-free solder.

The invention introduces a sufficient amount of copper in the solder above the barrier layer to prevent this unwanted diffusion. This significantly reduces the diffusion of elemental copper through the barrier layer. In effect, the introduction of copper reduces the chemical potential gradient of copper across the barrier layer. Reduction of this chemical potential gradient decreases the diffusive flux of elemental copper through the barrier layer, even at elevated temperatures. In this manner, the serviceability requirements of the application in question are consequently enhanced.

Thus, the invention controls the composition of the solder alloy (for the additional copper layer) to protect against voiding of BLM-layered structures and delamination to the diffusion of copper. This BLM barrier technology enables the use of higher current densities for advanced CMOS designs, and extends the reliability of current CMOS designs. Moreover, this technology is easily adopted by current methods for fabricating C4s.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood from the following detailed description with reference to the drawings, in which:

Figure 1 is a schematic diagram of an interconnect structure;

Figure 2 is a schematic diagram of an interconnect structure;

Figure 3 is a schematic diagram of an interconnect structure; and

Figure 4 is a schematic diagram of an interconnect structure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

The invention provides a structure that controls the composition of the solder alloy to protect against voiding of BLM-layered structures and delamination to the diffusion of copper, whether such diffusion is caused by self-diffusion or enhanced self-diffusion by such processes as electro-migration or thermo-migration. This BLM barrier technology enables the use of higher current densities for advanced CMOS designs, and extends the reliability of current CMOS designs. Moreover, this technology is easily adopted by current methods for fabricating C4s.

As explained above, C4 bump BLM structures are susceptible to reliability failures in the ball-limiting metallurgy (BLM) when used to support tin-containing solders because the copper will diffuse through the barrier metallurgy and into the solder, leaving the layer of copper voided and depleted. This migration of the BLM copper is driven by the chemical potential gradient across the barrier layer, which results because elemental copper is unstable in the presence of tin, preferring to form intermetallic compounds such as Cu_3Sn or $\text{Cu}(\text{Ni})_6\text{Sn}_5$.

The invention introduces a sufficient amount of copper in the solder above the barrier layer to prevent this unwanted diffusion. This significantly reduces the diffusion of elemental copper through the barrier layer. In effect, the introduction of copper reduces the chemical

potential gradient of copper across the barrier layer. Reduction of this chemical potential gradient decreases the diffusive flux of elemental copper through the barrier layer, even at elevated temperatures. In this manner, the serviceability requirements of the application in question are consequently enhanced.

Figure 1 illustrates a C4 BLM interconnect structure that is formed on an external portion of the structure (e.g., substrate) 1. These interconnects have a metal layer 2 on the substrate, a first copper layer 3 on the metal layer 2, a barrier layer 4 on the copper layer 3, and a tin-based solder bump 5 on the barrier layer. The metal layer 2 comprises diffusion metallurgy including one or more of Al, Ti, TiW, Cr, Ta, and TaN. The barrier layer 4 can be Ni, V, or NiV. The tin-based solder bump 5 can be either a eutectic PbSn solder or a lead-free solder.

As discussed above, the copper 3 is strongly attracted to the solder bump 5 because of the chemical potential gradient. If the copper 3 diffuses across the barrier layer 4 into the solder bump 5, this will create voids within the copper layer 3, which substantially increases the likelihood of delamination.

Figure 2 illustrates the addition of a stabilizing copper layer 6 that has a sufficient amount of copper to balance the chemical potential gradient of copper across the barrier layer and prevent copper within the first copper layer from diffusing across the barrier layer. After annealing processes, some of the copper diffuses from layer 6 into the solder bump 7. Thus, the tin-based solder bump 7 comprises a copper rich solder alloy.

Alternatively, as shown in Figure 3 a sufficient amount of copper can be included within the tin-based solder bump 8 to prevent copper from diffusing across the barrier layer, thereby eliminating the need for a distinct, separate copper layer 6. Additionally, if desired, as shown in

Figure 4, the invention can include the tin-based solder bump 8 and a separate copper layer 6, depending upon the volume of copper required by the individual designer's requirements.

The addition of Cu to the solder 8 may be accomplished in several ways, including: directly alloying the solder before application to the BLM structure, plating Cu as part of the solder alloy onto the BLM structure or introducing a stabilizing Cu layer 6 over the barrier layer 4 before applying the Sn based solder. All of these methods enable the alloying of the solder with Cu. In doing so, the chemical potential of Cu is raised in the solder and the diffusion through the barrier layer is reduced.

During the reflow processing of the chip, the solder will dissolve substantial amounts of Cu from the stabilizing layer 6, thus raising the Cu content of the solder 7 and producing a Cu rich solder alloy. This increase in the Cu concentration in the solder dramatically decreases the Cu Diffusion through the barrier layer 4. Therefore, the invention substantially reduces the likelihood of voiding and delamination, which increases yield and reliability.

Thus, as shown above, the invention introduces a sufficient amount of copper in the solder above the barrier layer to prevent this unwanted diffusion. This significantly reduces the diffusion of elemental copper through the barrier layer. In effect, the introduction of copper reduces the chemical potential gradient of copper across the barrier layer. Reduction of this chemical potential gradient decreases the diffusive flux of elemental copper through the barrier layer, even at elevated temperatures. In this manner, the serviceability requirements of the application in question are consequently enhanced.

Thus, the invention controls the composition of the solder alloy (for the additional copper layer) to protect against voiding of BLM-layered structures and delamination to the diffusion of

copper. This BLM barrier technology enables the use of higher current densities for advanced CMOS designs, and extends the reliability of current CMOS designs. Moreover, this technology is easily adopted by current methods for fabricating C4s.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.